LISTING OF CLAIMS

This listing of claims replaces all prior versions and listings of claims in the application per MPEP 714:

1. (currently amended) A method of generating a precharge pulse, comprising:

initiating charging of the precharge pulse at a first edge of a first clock-like signal; and

ending the charging of the precharge pulse after a time period that is longer of one of a preset delay period and a time period designated by a second edge of a second clock-like signal, wherein ending the charging of the precharge pulse after a time period that is longer of one of a preset delay period and a time period designated by a second edge of the second clock-like signal includes,

transmitting the first clock-like signal to a first NAND gate;

contemporaneously transmitting the second clock-like signal to a second NAND gate;

transmitting an output of the second NAND gate to the first NAND gate and an inverter; and

maintaining a charging state according to an output from the first NAND gate and the inverter.

2. (original) A method of generating a precharge pulse as recited in claim 1, wherein the first edge is a rising edge and the second edge is a falling edge.

3. (original) A method of generating a precharge pulse as recited in claim 1, wherein the precharge pulse initiates the precharging of bitlines.

4. (canceled)

5. (currently amended) A method of generating a precharge pulse as recited in claim ~~4~~ 1, wherein the precharge pulse shape/width is determined by the latter of the second edge of the second clock-like signal and an end of ~~the~~ a self-timed pulse.

6. (original) A method of generating a precharge pulse as recited in claim 1, wherein the precharging ends when the precharge pulse ends.

7. (currently amended) A method of generating a precharge pulse as recited in claim ~~4~~ 1, wherein a self-timed pulse is a minimum precharge pulse width.

8. (currently amended) A method of generating a precharge pulse as recited in claim 1, wherein the second edge of the second clock-like signal is the maximum precharge pulse width.

9. (original) A method of generating a precharge pulse as recited in claim 1, wherein the first edge is a falling edge and the second edge is a rising edge.

10. (previously presented) A precharge circuit capable of generating a precharge pulse, comprising:

circuitry for initiating charging of the precharge pulse at a first edge of a first clock-like signal; and

circuitry for ending the charging of the precharge pulse after a time period that is longer of one of a preset delay period and a time period designated by a second edge of a second clock-like signal, the circuitry for ending the charging of the precharge pulse including,

a first NAND gate coupled to a gate of a P-type transistor;

a second NAND gate coupled to the first NAND gate and an inverter; the inverter coupled to a gate of an N-type transistor; and

a storage element in electrical communication with the P-type transistor and the N-type transistor.

11. (original) A precharge circuit as recited in claim 10, wherein the first edge is a rising edge and the second edge is a falling edge.

12. (original) A precharge circuit as recited in claim 10, wherein the precharge pulse initiates the precharging of bitlines.

13. (original) A precharge circuit as recited in claim 12, wherein the preset delay period is determined by a self-timed pulse.

14. (currently amended) A precharge circuit as recited in claim 13, wherein the precharge pulse shape/width is determined by the latter of the second edge of the second clock-like signal and an end of the self-timed pulse.

15. (original) A precharge circuit as recited in claim 10, wherein the precharging ends when the precharge pulse ends.

16. (original) A precharge circuit as recited in claim 13, wherein the self timed pulse is a minimum precharge pulse width.

17. (previously presented) A precharge circuit as recited in claim 10, wherein the second edge of the second clock-like signal is the maximum precharge pulse width.

18. (previously presented) A precharge circuit as recited in claim 10, further comprising:

circuitry for receiving the precharge pulse and generating a precharge for a time corresponding to the duration of the precharge pulse.

19. (previously presented) A method of generating a precharge pulse, comprising:

initiating charging of the precharge pulse at a first edge of a first clock-like signal; and

ending the charging of the precharge pulse after a time period that is longer of one of a preset delay period and a time period designated by a second edge of a second clock-like signal, the preset delay period being determined by a self-timed pulse; ending the charging further including,

transmitting the first clock like signal to a first NAND gate;

contemporaneously transmitting the second clock like signal to a second NAND gate;

transmitting an output of the second NAND gate to the first NAND gate and an inverter; and

maintaining a charging state according to an output from the first NAND gate and the inverter.

wherein the precharge pulse initiates the precharging of bitlines and the precharging terminates when the precharge pulse ends.

20. (original) A method of generating a precharge pulse as recited in claim 19, wherein the first edge is a rising edge and the second edge is a falling edge.

21. (previously presented) A method of generating a precharge pulse as recited in claim 19, wherein the precharge pulse width is determined by the latter of the second edge of the second clock-like signal and an end of the self-timed pulse.

22. (original) A method of generating a precharge pulse as recited in claim 19, wherein the self timed pulse is a minimum precharge pulse width.

23. (currently amended) A method of generating a precharge pulse as recited in claim 19, wherein the second edge of the second clock-like signal is a maximum precharge pulse width.

24. (original) A method of generating a precharge pulse as recited in claim 19, wherein the first edge is a falling edge and the second edge is a rising edge.